Display LED matrix
7 x 8

LED

Typ 7 pl.

R3
47R

F2A
7406

Q1
2N1311
VCC

Typ 8 pl.
R2
470R

MONA
MONB
MONC
MOND
MONE
MONF
MONG

D6A
74100
IQ1 I0
2Q1 I4
1IC I1
2Q2 I5
1D2
2D2

D6B
74100
IQ3 I2
2Q3 I6
2IC
2D3 I3
1Q4 I7
2D4

B6C
7427

Instruction Register

TSB0
TSB4
TSB1
TSB5
BETA
BOX1
LSB
TSB2
TSB6
TSB3
TSB7

D2
7472
PRE
I1
I3
CLK
K1
K2
K3
CLR
Q
Q
SIG

VCC

B2C
7400

F5
7442
A0
A1
A2
A3

E4A
9601
RCext 2mS
Cext
A
B
C
D
Q
Q

R1
12k
C1
0.47u
VCC

Safety catch
Intercepts
clock failure

A5A
7474
CB
D   Q
CLK
SD Q

A4C
7410

A4B
7410

B6B
7427

Internal Carry

CSET
LSB
COUT
BETA
LSB
ALPHA

A4A
7410
VCC
GAMMA

GAMMA

I6
I4
GAMMA
I7
BOX27
RESET*

D5
74151
I0
I1
I2
I3
I4
I5
I6
I7
A
B
C
E
Z
Z
MOND
ADDR13*
ADDR12*
ADDR11*

D1
74151
L0
L1
L2
N
CA
CB
SIG
A
B
C
E
Z
Z
MONG
ADDR13*
ADDR12*
ADDR11*

ADDR13*
ADDR12*
ADDR11*

P1
60PIN
1 GND
2 VCC
3 RESET*
4 ALPHA
5 BETA
6 GAMMA
7
8 PHASE2
9 INTREQ*
10 LSB
11 BOX25
12 BOX26
13 BOX27
14 BOX29
15 BOX21
16 BOX12
17 REGSELA
18 CB
19 Z1IN
20 F0
21 COUT
22 MONC
23 BOX31
24 SPD0
25 BOX28
26 SPD1
27 TC
28 MONF
29 MONE
30 SPAR0*
31 SPAR1*
32 SPAR2*
33 SPAR3*
34 SPAR0
35 PHASE2*
36 TSB0
37 TSB1
38 TSB2
39 TSB3
40 TSB4
41 TSB5
42 TSB6
43 TSB7
44 SENSE*
45 I0
46 I1
47 I2
48 I3
49 I7
50 MONA
51 TESTC
52 CSET
53 SPAR1
54 SPAR2
55 ADDR11*
56 ADDR12*
57 ADDR13*
58 SPAR3
59 BYTE
60 GND

P2
16PIN
A END
B INTLVL
C MANSEL
D BOX10
E REGSELB
F FORCINT
G
H ALPHA
J MPSTEP
K
L
M

Title
Size B
Number
Revision
Date: 11-Dec-1999
File: F:\WebSite Image\simplex\simplex.ddb
Sheet of
Drawn By: