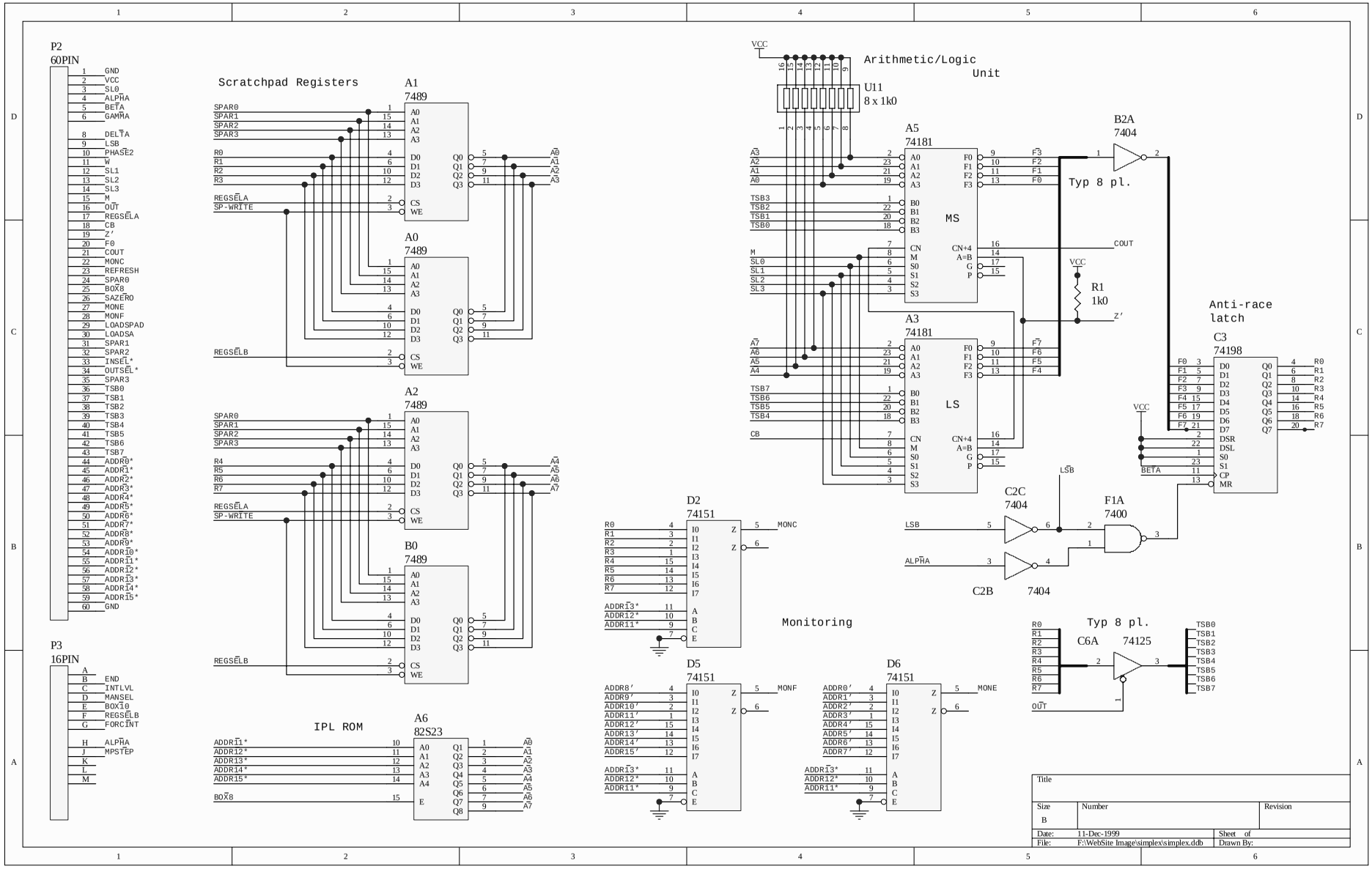
P2
60PIN
1 GND
2 VCC
3 SL0
4 ALPHA
5 BETA
6 GAMMA
8 DELTA
9 LSB
10 PHASE2
11 W
12 SL1
13 SL2
14 SL3
15 M
16 OUT
17 REGSELA
18 CB
19 Z'
20 F0
21 COUT
22 MONC
23 REFRESH
24 SPAR0
25 BOX8
26 SAZERO
27 MONE
28 MONF
29 LOADSPAD
30 LOADSA
31 SPAR1
32 SPAR2
33 INSEL*
34 OUTSEL*
35 SPAR3
36 TSB0
37 TSB1
38 TSB2
39 TSB3
40 TSB4
41 TSB5
42 TSB6
43 TSB7
44 ADDR0*
45 ADDR1*
46 ADDR2*
47 ADDR3*
48 ADDR4*
49 ADDR5*
50 ADDR6*
51 ADDR7*
52 ADDR8*
53 ADDR9*
54 ADDR10*
55 ADDR11*
56 ADDR12*
57 ADDR13*
58 ADDR14*
59 ADDR15*
60 GND
P3
16PIN
A
B END
C INTLVL
D MANSEL
E BOX10
F REGSELB
G FORCINT
H ALPHA
J MPSTEP
K
L
M
Scratchpad Registers
A1
7489
A0
7489
A2
7489
B0
7489
SPAR0
SPAR1
SPAR2
SPAR3
R0
R1
R2
R3
R4
R5
R6
R7
REGSELA
SP-WRITE
REGSELB
CS
WE
D0
D1
D2
D3
Q0
Q1
Q2
Q3
A0
A1
A2
A3
A4
A5
A6
A7
IPL ROM
A6
82S23
ADDR11*
ADDR12*
ADDR13*
ADDR14*
ADDR15*
BOX8
E
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
VCC
U11
8 x 1k0
Arithmetic/Logic
Unit
A5
74181
MS
A3
74181
LS
B2A
7404
Typ 8 pl.
COUT
R1
1k0
Z'
Anti-race
latch
C3
74198
DSR
DSL
S0
S1
CP
MR
BETA
LSB
C2C
7404
F1A
7400
ALPHA
C2B
7404
D2
74151
MONC
Monitoring
D5
74151
MONF
D6
74151
MONE
C6A
74125
OUT
TSB0
TSB1
TSB2
TSB3
TSB4
TSB5
TSB6
TSB7
Title
Size
B
Number
Revision
Date: 11-Dec-1999
Sheet of
File: F:\WebSite Image\simplex\simplex.ddb
Drawn By: